# Personal Line Logic Analyzer System

- Microsoft Windows* 3.1x and Windows 95 Interface
- Disassemblers Require No Preprocessors
- High Level Language Debugging
- Trigger on Source Code Line
- 32K Memory Depth with Full Channel Count, 64K at Half the Channels
- High Impedance 16 Channel Active Logic Probes
- Internal Clock Rates Up to 1 GHz for 72 Channels or 500 MHz with 144 Channels
- 32 to 192 Channels with External Clock Rate of 100 MHz
- 15 Level Trigger with Physical Trigger Outputs to Trigger External Devices

A full range of Disassembler and High Level Language support enables the Personal Line Logic Analyzer Family to be used as a very flexible and powerful Soft- and Hardware development tool for all Embedded Intel Microprocessors. This is backed up by dli's "Flexible Adaption" feature, which allows the recording of the necessary signals either directly from the Microprocessor pins (if the package allows it) or from any other pin within the system. As this flexible support does not require Microprocessor package specific parts, all new Microprocessor versions containing the same core, are supported with no or only small modifications of the already existing Disassemblers and High Level Language converters.

Capabilities include full time-correlated dual processor tracing (expandable to 32 processors), a Software Interface to control and operate the Personal Line from user written programs, and a 10 ns Time Stamp for time correlation of all processors being monitored.

PROCESSORS SUPPORTED:
80186/80188, 80C186XL/80C188XL, 80C186EA/80C188EA, 80C186EB/80C188EB, 801186EB/801188EB, 80C186EC/80C188EC, 801186EC/801188EC, i386™ EX/CXSA, CXSB/DX/SX/SXSA; Intel486™ and Pentium® processors 100/133/166 MHz

DEVELOPMENT PLATFORMS:
PC Windows 3.11, Windows 95

AVAILABILITY:
Now

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